WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

an internal circuit;

a signal transmission line coupled between said internal circuit and a pad, for transmitting a high frequency signal between said pad and said internal circuit;

a bypass transmission line connected between a first node of said signal transmission line and a first power supply node, for transmitting at least a signal component that is higher in frequency than said high frequency signal; and

a first surge conducting element connected between a second node of said signal transmission line and said first power supply node, for causing a current to flow between said second node and said first power supply node when a voltage at said first node exceeds a prescribed voltage level, said second node being provided between said first node and said internal circuit.

2. The semiconductor device according to claim 1, wherein said first surge conducting element includes a PN junction coupled in a reverse direction viewed from said second node toward said first power supply node.

3. The semiconductor device according to claim 1, wherein said first surge conducting element includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to said first power supply node, and a second conduction node connected to said second node.

4. The semiconductor device according to claim 1, wherein said first surge conducting element includes a diode element connected in a reverse direction viewed from said second node.

5. The semiconductor device according to claim 1, further

comprising a second surge conducting element connected between a third node of said signal transmission line and a second power supply node, and rendered conductive when a voltage at said third node exceeds a voltage level applied in a normal operation, said third node being provided on said signal transmission line between said first node and said internal circuit.

6. The semiconductor device according to claim 5, wherein said second surge conducting element includes a PN junction coupled in a reverse direction viewed from said third node toward said second power supply node.

7. The semiconductor device according to claim 5, wherein said second surge conducting element includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to said second power supply node, and a second conduction node connected to said third node.

8. The semiconductor device according to claim 5, wherein said second surge conducting element includes a diode element connected to said third node in a reverse direction viewed from said third node.

9. The semiconductor device according to claim 1, further comprising a capacitor connected between said second node and said internal circuit.

10. The semiconductor device according to claim 1, further comprising a clamp circuit connected between said first power supply node and a second power supply node, for holding a voltage difference between the first and second power supply nodes so as not to exceed a prescribed voltage level.

11. The semiconductor device according to claim 10, wherein said clamp circuit clamps said voltage difference between said first and second

power supply nodes to a voltage level lower than a breakdown voltage of a diffusion layer of a second conductivity type formed on a surface of a substrate region of a first conductivity type.

12. The semiconductor device according to claim 10, wherein said clamp circuit includes an insulated-gate field effect transistor having a gate, a first conduction node and a back gate connected together to said first power supply node, and a second conduction node connected to said second power supply node.

13. The semiconductor device according to claim 10, wherein said clamp circuit includes an insulated-gate field effect transistor having a gate, a back gate and a first conduction node connected together to said second power supply node, and a second conduction node connected to said first power supply node.

14. The semiconductor device according to claim 10, wherein said clamp circuit includes at least one first diode element connected between said first power supply node and said second power supply node in a forward direction viewed from said first power supply node, and at least one second diode element connected between said second power supply node and said first power supply node in a forward direction viewed from said second power supply node.

15. The semiconductor device according to claim 1, wherein said first power supply node is a ground node.

16. The semiconductor device according to claim 1, wherein said bypass transmission line is a quarter wavelength transmission line having a length substantially equal to a quarter of an effective wavelength of an operation frequency of said internal circuit.